Claims

What is claimed is:

1. A fully symmetrical current amplifier comprising:

two inputs and a plurality of outputs,

first means for amplifying such that a first input is responsive to a current signal;

second means for amplifying such that a second input is responsive to a current signal;

third means for biasing such that voltage and current offset can be reduced to approximately zero;

wherein said first input and said second input possess substantially equal properties;

wherein there is at least one input, inverting input, for which at least one output produces a signal in response to a signal at said inverting input that is 180° out of phase with said input signal at said inverting input;

whereby the amplifier can use negative feedback;

whereby the amplifier can use techniques normally associated with Current Feedback Amplifiers; and

whereby improved performance can be realized while using less complex circuitry.

2. A fully symmetrical current amplifier comprising:

two inputs and two outputs, where outputs are designated first and second output;

fourth means for amplifying such that a first input is responsive to a current signal;

fifth means for amplifying such that a second input is responsive to a current signal;

sixth means for biasing such that voltage and current offset can be reduced to approximately zero;

wherein said first input and said second input possess substantially equal properties;

wherein there is at least one input, inverting input, for which at least one output produces a signal in response to a signal at said inverting input that is 180° out of phase with said input signal at said inverting input;

whereby the amplifier can use negative feedback;

whereby the amplifier can use techniques normally associated with Current Feedback Amplifiers; and

whereby improved performance can be realized while using less complex circuitry.

3. A fully symmetrical current amplifier comprising:

two inputs and one output, , where outputs are designated first and second output;

seventh means for amplifying such that a first input is responsive to a current signal;

eighth means for amplifying such that a second input is responsive to a current signal;

ninth means for biasing such that voltage and current offset can be reduced to approximately zero;

wherein said first input and said second input possess substantially equal properties;

wherein there is at least one input, inverting input, for which the output produces a signal in response to a signal at said inverting input that is 180° out of phase with said input signal at said inverting input;

whereby the amplifier can use negative feedback;

whereby the amplifier can use techniques normally associated with Current Feedback Amplifiers; and

whereby improved performance can be realized while using less complex circuitry.

4. The amplifier as set forth in claim 2 wherein:

increasing current into said first input produces decreasing current in said first output and increasing current into said second input produces decreasing current in said second output and decreasing current into said first input produces increasing current in said first output and decreasing current into said second input produces increasing current in said second output;

increasing current into said first input produces increasing current in said second output and increasing current into said second input produces increasing current in said first output and decreasing current into said first input produces decreasing current in said second output and decreasing current into said second input produces decreasing current in said first output; and

whereby said association of said first input to said first output and said second input to said second output will be called an inverting relationship and the relationship of said first input to said second output and said second input to said first output will be called a non-inverting relationship;

whereby said amplifier produces a current between the said first and second outputs proportional to the current difference between said first and second inputs, such output current difference can travel via ground and power supplies.

5. The amplifier as set forth in claim 3:

wherein increasing current into first input produces decreasing current in said output and increasing current into second input produces increasing current in said output and similarly decreasing current into said first input produces increasing current in said output and decreasing current into said second input produces decreasing current in said output;

whereby said association of said first input to said output will be called an inverting relationship and the relationships of said second input to said output will be called a non-inverting relationship;

whereby said amplifier produces a current output proportional to the current difference between said second and first inputs.

6. The amplifier as set forth in claim 4 comprising:

two NPN transistors, two PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
the collector of first NPN transistor is connected to the collector of said second PNP transistor and,
the bases of second NPN transistor and second PNP transistor are connected and,
the collector of said second NPN transistor is connected to the collector of said second PNP transistor and,
the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,

the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and;

whereby the connection of said bases of said first NPN transistor and first PNP transistor can be referred to as said first input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said second input, and

the connection of the said collectors of said first NPN transistor and said first PNP transistor can be referred to as said first output and the connection of said collectors of said second NPN transistor and said second PNP transistor can be referred to as said second output, and

whereby the amplifier is a fully differential amplifier of a simple design.

7. The amplifier as set forth in claim 4 comprising:

four NPN transistors, four PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
said first NPN transistor collector is connected to the base of third PNP transistor where emitter of said third PNP transistor is connected to a positive voltage supply and,
said first PNP transistor collector is connected to the base of third NPN transistor where emitter of said third NPN transistor is connected to a negative voltage supply and,
the bases of second NPN transistor and second PNP transistor are connected and,
said second NPN transistor collector is connected to the base of fourth PNP transistor where emitter of said fourth PNP transistor is connected to a positive voltage supply and,
said second PNP transistor collector is connected to the base of fourth NPN transistor where emitter of said fourth NPN transistor is connected to a negative voltage supply and,

the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,
the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and,
collectors of said third NPN transistor and said third PNP transistor are connected together and,
collectors of said fourth NPN transistor and said fourth PNP transistor are connected together;

whereby the connection of said bases of said first NPN transistor and first PNP transistor can be referred to as said first input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said second input, and

the connection of the said collectors of said third NPN transistor and said third PNP transistor can be referred to as said second output and the connection of said collectors of said fourth NPN transistor and said fourth PNP transistor can be referred to as said first output, and

whereby the amplifier is a fully differential amplifier of a simple design with high performance that can be operated from low voltage supplies of less than .75 volts plus and minus.

8. The amplifier as set forth in claim 2 further including tenth means for isolating said first output and said second output from external loads;

said tenth means would include the use of buffer amplifiers between the said first and said second outputs and any loads being driven by said first and said second outputs;

whereby a practitioner of the art could more closely control the response of the amplifier.

9. The amplifier as set forth in claim 8 further including eleventh means for converting internally each of said first output and said second output from a current to a voltage, to allow for compensation of loop gain and frequency response of the amplifier while isolating said first output and said second output from external loads;

said eleventh means would include the use of an impedance to ground at each of said first output and said second output and the inclusion of buffer amplifiers between the said first and second outputs and any loads being driven by said outputs;

whereby the outputs at said loads, buffered outputs, would be in the form of a voltage rather than a current;

whereby a practitioner of the art could more closely control the response of the amplifier by choosing the impedance at said first and said second outputs.

10. The amplifier as set forth in claim 8 comprising:

two current sources, 10 NPN transistors and 10 PNP transistors;

wherein said transistors, said current sources and supply voltages are connected as detailed in Figure 10;

wherein said first and said second outputs are marked as E and F and are internal summing/compensation points of the amplifier and any impedances connected to said points E and F create a voltage at said points E and F and said impedances alter the gain of the amplifier;

wherein output at said loads is a voltage rather than a current.

11. The amplifier as set forth in claim 2 wherein:

increasing current into said first input produces decreasing current in both said first output and said second output and increasing current into said second input produces increasing current in both said first output and said second output and,
decreasing current into said first input produces increasing current in both said first output and said second output and decreasing current into said second input produces decreasing current in both said first output and said second output;

whereby association of said first input to said first output will be called an inverting relationship and association of said second input to said second output will be called an non-inverting relationship.

12. The amplifier as set forth in claim 11 comprising:

three NPN transistors, three PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
said first NPN transistor collector is connected to the base of third PNP transistor where emitter of said third PNP transistor is connected to a positive voltage supply and,
said first PNP transistor collector is connected to the base of third NPN transistor where emitter of said third NPN transistor is connected to a negative voltage supply and,
the bases of second NPN transistor and second PNP transistor are connected and,
the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,
the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and,
collectors of said first NPN transistor and said first PNP transistor are connected together and,
collectors of said third NPN transistor and said third PNP transistor are connected together and;

the connection of said bases of said first NPN transistor and said first PNP transistor can be referred to as said second input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said first input and,
the connection of the said collectors of said third NPN transistor and said third PNP transistor can be referred to as said second output and the connection of said collectors of said second NPN transistor and said second PNP transistor can be referred to as said first output.

13. The amplifier as set forth in claim 11 further including:

twelfth third means for compounding the gains of the two sections of the amplifier and eliminate one input and one output;

said twelfth means would include connecting said first output to said second input;

said twelfth means would include an impedance network, a plurality of impedances connected in series and parallel to ground, connected between the said first output and said second input;

whereby a practitioner of the art could more closely control of the open loop frequency response of the amplifier;

whereby such a amplifier would have an inverting input and an output, would be referenced only by current until the load is connected in some forcing manner to a voltage reference such as ground;

whereby one can direct negative feedback from the resulting output, said second output, to the resulting inverting input, said first input, to establish a fixed closed loop gain for the amplifier;

whereby the amplifier is no longer affected by a high-gain non-inverting input, which in prior amplifier designs could introduce hum and interference.

14. The amplifier as set forth in claim 2 further including:

thirteenth means for deactivating one of the two said outputs of the said amplifier;

said thirteenth means would include connecting one of said outputs to a low-impedance point, such low impedance point includes, but not limited to, ground and power supply terminals;

whereby the amplifier is easier to use when driving a load to ground.

15. The amplifier as set forth in claim 5 further including:

fourteenth means for isolating said output from an external load;

said fourteenth means would include the use of a buffer stage between said output and an external load;

said fourteenth means could also include the use of an impedance to ground at the said output to produce a voltage at said point;

whereby the output at said load could be in the form of a voltage rather than a current;

whereby said inputs would still be controlled by current rather than voltage thus preserving the benefits of the amplifier topologies;

whereby by the use of series impedances, external voltages could be seen as a currents by said inputs.

16. The amplifier as set forth in claim 5 comprising:

two NPN transistors, two PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
the collector of said first NPN transistor is connected to a negative supply voltage, and
the collector of said second PNP transistor is connected to a positive supply voltage and,
the bases of second NPN transistor and second PNP transistor are connected and,
the collector of said second NPN transistor is connected of the collector of said second PNP transistor and,
the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,
the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and;

whereby the connection of said bases of said first NPN transistor and first PNP transistor can be referred to as said first input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said second input and,
the connection of the said collectors of said second NPN transistor and said second PNP transistor can be referred to as said output.

17. The amplifier as set forth in claim 5 comprising:

three NPN transistors, three PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
said first NPN transistor collector is connected to the base of third PNP transistor where emitter of said third PNP transistor is connected to a positive voltage supply and,
said first PNP transistor collector is connected to the base of third NPN transistor where emitter of said third NPN transistor is connected to a negative voltage supply and,
the bases of second NPN transistor and second PNP transistor are connected and,
said second NPN transistor collector is connected to the positive voltage supply and,
said second PNP transistor collector is connected to the negative voltage supply,

the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,
the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and,
collectors of said third NPN transistor and said third PNP transistor are connected together;

whereby the connection of said bases of said first NPN transistor and first PNP transistor can be referred to as said first input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said second input and,
the connection of the said collectors of said third NPN transistor and said third PNP transistor can be referred to as said output.

18. The amplifier as set forth in claim 13 further including:

fifteenth means for converting internally said output from a current to a voltage, to allow for compensation of loop gain and frequency response of the amplifier while isolating said output from an external load;

said fifteenth means would include the use of an impedance to ground at said output and a buffer amplifier between the said output and a load being driven;

whereby the output signal at the said load would be in the form of a voltage rather than a current;

whereby a practitioner of the art could more closely control the response of the said amplifier.

19. The amplifier as set forth in claim 18 comprising:

two current sources, 6 NPN transistors and 6 PNP transistors;

wherein said transistors, said current sources and supply voltages are connected as detailed in Figure 9;

wherein said sixth means would include the connection of an impedance from point marked F to ground;

wherein output signal at said load is a voltage rather than a current.

20. The amplifier as set forth in claim 4 further including sixteenth means for establishing the quiescent current of all the transistors to be substantially the same;

wherein sixteenth seventh means would include the use of current mirrors;

whereby the closed loop frequency response of the circuit is increased at the expense of loop gain;

whereby the circuit would have ease of loop gain compensation.

21. The amplifier as set forth in claim 20 comprising:

six NPN transistors, six PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
said first NPN transistor collector is connected to the bases of third and fifth PNP transistors where emitters of said third and fifth PNP transistors are connected to a positive voltage supply and,
said first PNP transistor collector is connected to the base of third and fifth NPN transistors where emitters of said third and fifth NPN transistors are connected to a negative voltage supply and,
the bases of second NPN transistor and second PNP transistor are connected and,
said second NPN transistor collector is connected to the base of fourth and sixth PNP transistors where emitters of said fourth and sixth PNP transistors are connected to a positive voltage supply and,
said second PNP transistor collector is connected to the base of fourth and sixth NPN transistors where emitters of said fourth and sixth NPN transistors are connected to a negative voltage supply and,

the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,

the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and,
collectors of said fifth and sixth NPN transistors are connected to the bases of self said transistor and,
collectors of said fifth and sixth PNP transistors are connected to the bases of self said transistors and,
collectors of said third NPN transistor and said third PNP transistor are connected together and,
collectors of said fourth NPN transistor and said fourth PNP transistor are connected together;

whereby the connection of said bases of said first NPN transistor and first PNP transistor can be referred to as said first input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said second input and,
the connection of the said collectors of said third NPN transistor and said third PNP transistor can be referred to as said second output and the connection of said collectors of said fourth NPN transistor and said fourth PNP transistor can be referred to as said first output.

22. The amplifier as set forth in claim 1 further including seventeenth means for converting an external signal voltage input to an input current to said amplifier and eighteenth means for converting said amplifier output current to a voltage;

wherein said seventeenth means would include a series input impedance to a plurality of said inputs; and

wherein eighteenth means would include a parallel output impedance to ground;

whereby amplifier could then be responsive to voltages while still operating in the current domain.

23. The amplifier of claim 2 further including nineteenth means for supplying negative current feedback to the amplifier;

wherein said nineteenth means would include a feedback impedance from said first output to said first current input and from said second output to said second current input;

thereby with the use of an input resistor one realizes a predictable fixed voltage closed loop gain.

24. The amplifier as set forth in claim 1 wherein said means comprising:

four NPN transistors, four PNP transistors and two current sources;

wherein the bases of first NPN transistor and first PNP transistor are connected and,
said first NPN transistor collector is connected to the base of third PNP transistor where emitter of said third PNP transistor is connected to a positive voltage supply and,
said first PNP transistor collector is connected to the base of third NPN transistor where emitter of said third NPN transistor is connected to a negative voltage supply and,
the bases of second NPN transistor and second PNP transistor are connected and,
said second NPN transistor collector is connected to the base of fourth PNP transistor where emitter of said fourth PNP transistor is connected to a positive voltage supply and,
said second PNP transistor collector is connected to the base of fourth NPN transistor where emitter of said fourth NPN transistor is connected to a negative voltage supply and,

the emitters of said first PNP transistor and said second PNP transistor are connected together to one terminal of a first constant current source which is connected to a positive voltage supply and,
the emitters of said first NPN transistor and said second NPN transistor are connected together to one terminal of a second constant current sink which is connected to a negative voltage supply and,
collectors of said third NPN transistor and said third PNP transistor are connected together and,
collectors of said fourth NPN transistor and said fourth PNP transistor are connected together;

whereby the connection of said bases of said first NPN transistor and first PNP transistor can be referred to as said first input and the connection of said bases of said second NPN transistor and second PNP transistor can be referred to as said second input, and
the connection of the said collectors of said third NPN transistor and said third PNP transistor can be referred to as a second output and the connection of said collectors of said fourth NPN transistor and said fourth PNP transistor can be referred to as a first output, and

whereby the amplifier is a fully differential current amplifier of a symmetrical and simple design with high performance that can be operated from low voltage supplies of less than .75 volts plus and minus.